

CLAIMS

1 1. (currently amended) A method for processing a data signal, comprising:
2 transmitting ~~the~~ an original data signal through an electrical backplane or through the electrical
3 backplane and at least one filter, wherein:
4 the original data signal is a binary data signal; and
5 the transfer function property of the electrical backplane or the transfer function property
6 of the combination of the electrical backplane and the at least one filter corresponds to the transfer
7 function property of a binary-to-duobinary converter; and
8 receiving the data signal after being transmitted through the electrical backplane or through the
9 electrical backplane and the at least one filter, wherein the received data signal is ~~interpreted~~ processed
10 as a duobinary data signal.

1 2. (currently amended) The invention of claim 1, further comprising precoding an input
2 binary data signal, wherein the original data signal transmitted through the electrical backplane is based
3 on the precoded binary data signal.

1 3. (currently amended) The invention of claim 1, further comprising filtering the data
2 signal using the at least one filter prior to ~~interpreting~~ processing the received data signal as the
3 duobinary data signal.

1 4. (original) The invention of claim 3, wherein the filtering is implemented before
2 transmission through the electrical backplane.

1 5. (original) The invention of claim 3, wherein the filtering comprises equalizing filtering.

1 6. (original) The invention of claim 3, wherein the filtering is designed to emphasize high-
2 frequency components in the data signal and flatten group delay of the electrical backplane.

1 7. (original) The invention of claim 3, wherein the filtering is implemented using an FIR
2 filter.

1 8. (original) The invention of claim 3, wherein the filtering:
2 delays a first copy of the data signal;
3 attenuates the delayed first copy; and

4 adds the delayed first copy to a second copy of the data signal to generate the filtered data signal.

1 9. (original) The invention of claim 3, wherein the combination of the filtering and the
2 transmission through the electrical backplane approximates binary-to-duobinary conversion.

1 10. (currently amended) The invention of claim 1, wherein duobinary-to-binary (D/B)
2 conversion is applied to the received data signal to generate an output binary data signal.

1 11. (original) The invention of claim 10, wherein the D/B conversion comprises:
2 comparing amplitude of the received data signal with first and second threshold voltages to
3 generate first and second binary streams; and
4 applying a logic function to the first and second binary streams to generate the output binary data
5 signal.

1 12. (original) The invention of claim 11, wherein the logic function comprises an
2 exclusive-OR (XOR) function.

1 13. (original) The invention of claim 11, wherein the logic function comprises an
2 exclusive-NOR (XNOR) function.

1 14. (currently amended) The invention of claim 11, wherein:
2 the output data signal is an NRZ binary data signal; and
3 the first and second threshold voltages are selected such that one of the first and second binary
4 streams is always zero or always one.

1 15. (original) The invention of claim 1, wherein the electrical backplane comprises a multi-
2 layer board.

1 16. (currently amended) The invention of claim 1, further comprising:
2 precoding an input binary data signal, wherein the original data signal transmitted through the
3 electrical backplane is based on the precoded binary data signal;
4 filtering the data signal using the at least one filter prior to ~~interpreting~~ processing the received
5 data signal as the duobinary data signal; and

6 applying duobinary-to-binary conversion to the received data signal to generate an output binary
7 data signal.

1 17. (currently amended) The invention of claim 16, wherein:
2 the combination of the filtering and the transmission through the electrical backplane
3 approximates binary-to-duobinary conversion; and
4 the duobinary-to-binary conversion comprises:
5 comparing amplitude of the received data signal with first and second threshold voltages
6 to generate first and second binary streams; and
7 applying a logic function to the first and second binary streams to generate the output
8 binary data signal.

1 18. (currently amended) A transmission system for a data signal, comprising:
2 a transmitter subsystem adapted to transmit ~~the~~ an original data signal through an electrical
3 backplane or through the electrical backplane and at least one filter, wherein:
4 the original data signal is a binary data signal; and
5 the transfer function property of the electrical backplane or the transfer function property
6 of the combination of the electrical backplane and the at least one filter corresponds to the transfer
7 function property of a binary-to-duobinary converter; and
8 a receiver subsystem adapted to receive the data signal after being transmitted through the
9 electrical backplane or through the electrical backplane and the at least one filter, wherein the received
10 data signal is ~~interpreted~~ processed as a duobinary data signal.

1 19. (currently amended) The invention of claim 18, further comprising ~~a~~ the at least one
2 filter adapted to filter the data signal prior to the received data signal being ~~interpreted~~ processed as the
3 duobinary data signal.

1 20. (currently amended) The invention of claim 19, wherein the at least one filter is
2 designed to emphasize high-frequency components in the data signal and flatten group delay of the
3 electrical backplane.

1 21. (currently amended) The invention of claim 19, wherein the at least one filter comprises:
2 one or more delays adapted to delay a first copy of the data signal;
3 an attenuator adapted to attenuate the delayed first copy; and

4 a summing node adapted to add the attenuated, delayed first copy to a second copy of the data
5 signal to generate the filtered data signal.

1 22. (currently amended) The invention of claim 21, wherein the at least one filter further
2 comprises a selector connected to receive an output from each of a plurality of delays and adapted to
3 select one of the delay outputs as the signal applied to the attenuator.

1 23. (currently amended) The invention of claim 19, wherein the combination of the at least
2 one filter and the electrical backplane approximates a binary-to-duobinary converter.

1 24. (currently amended) The invention of claim 18, wherein the receiver subsystem
2 comprises a duobinary-to-binary (D/B) converter adapted to apply duobinary-to-binary conversion to the
3 received data signal to generate an output binary data signal.

1 25. (currently amended) The invention of claim 24, wherein the D/B converter comprises:
2 a splitter adapted to split the received data signal;
3 two comparators, each adapted to compare a copy of the received data signal to a specified
4 threshold voltage; and
5 a logic gate adapted to generate the output binary data signal from outputs from the two
6 comparators.

1 26. (currently amended) The invention of claim 25, wherein:
2 the output binary data signal is an NRZ binary data signal; and
3 the threshold voltages for the two comparators are selected such that one of the comparator
4 outputs is always zero or always one.

1 27. (currently amended) The invention of claim 18, wherein:
2 the transmitter subsystem comprises a precoder adapted to precode an input binary data signal,
3 wherein the original data signal transmitted through the electrical backplane is based on the precoded
4 binary data signal;
5 the system comprises ~~a~~ the at least one filter adapted to filter the data signal prior to the received
6 data signal being ~~interpreted~~ processed as the duobinary data signal; and
7 the receiver subsystem comprises a duobinary-to-binary converter adapted to apply duobinary-to-
8 binary conversion to the received data signal to generate an output binary data signal.

1 28. (currently amended) The invention of claim 27, wherein:
2 the combination of the at least one filter and the electrical backplane approximates a binary-to-
3 duobinary converter; and
4 the duobinary-to-binary converter comprises:
5 a splitter adapted to split the received data signal;
6 two comparators, each adapted to compare a copy of the received data signal to a
7 specified threshold voltage; and
8 a logic gate adapted to generate the output binary data signal from outputs from the two
9 comparators.

1 29. (currently amended) Apparatus for processing a data signal, comprising:
2 means for transmitting ~~the~~ an original data signal through an electrical backplane or through the
3 electrical backplane and at least one filter, wherein:
4 the original data signal is a binary data signal; and
5 the transfer function property of the electrical backplane or the transfer function property
6 of the combination of the electrical backplane and the at least one filter corresponds to the transfer
7 function property of a binary-to-duobinary converter; and
8 means for receiving the data signal after being transmitted through the electrical backplane or
9 through the electrical backplane and the at least one filter, wherein the received data signal is ~~interpreted~~
10 processed as a duobinary data signal.